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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/991,202	GOPINATH ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *26-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/26/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election filed on 12/16/04. Currently, claims 1-40 are pending.

Election/Restrictions

1. Applicant's election with traverse of 1-25 in the reply filed on 12/16/04 is acknowledged. The traversal is on the ground(s) that the inventions are not independent or distinct as claimed and that there is no serious burden on the Examiner. This is not found persuasive because the inventions I and II are distinctly related, resulting in patentably distinct inventions and requiring separate search areas. The requirement is still deemed proper and is therefore made FINAL.

2. Claims 26-40 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 12/16/04.

Information Disclosure Statement

3. The information disclosure statement (IDS) was submitted on 12/26/01. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

4. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: in figure 5, reference numbers "408" and "410". Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities: On page 7, lines 12-17 should be doubled spaced. On page 9, line 2, "8minutes" should read "8 minutes". Appropriate correction is required.

7. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: On pages 9-10, the specification does not clearly point out that the upper and lower dielectric layer combined would result in a dielectric constant less than silicon dioxide. For, example, on page 9, lines 10-11 and page 10, lines 1-2, respectively, the lower dielectric material (ex., carbon doped silicon oxide) has a dielectric constant 2.5 and the upper dielectric layer (ex., amorphous silicon carbide) has a dielectric constant of 5.0. The combined dielectric constants of the upper and lower dielectric layers results in a total dielectric constant of 7.5, where theses dielectric constants clearly do not equal to a dielectric constant less than silicon dioxide. Appropriate correction is required..

8. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 23 recites the limitation "the thickness of the first layer" and "the thickness of the second layer" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim. For examination purposes on the merits, the Examiner has regarded the "first layer" and the "second layer" as the "lower dielectric material" and the "upper dielectric material", respectively.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-5 and 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Fulford, Jr. et al. US Patent 6,008,109.

12. Fulford discloses the semiconductor method as claimed. See figures 1-11b, and corresponding text, where Fulford teaches pertaining to claim 1, a method of forming an isolation structure on an integrated circuit substrate, comprising: etching a trench **56** in the integrated circuit substrate (figure 3; col. 6, lines 33-36); forming a lower dielectric layer **64** in the trench, the lower dielectric layer partially filling the trench (figures 6a and 8a; col.7, lines 4-19, lines 25-43); and forming an upper dielectric layer **66** in the trench over the lower dielectric layer to create an isolation structure (figure 8a; col. 7, lines 47-50); wherein the upper dielectric layer has an HF etch rate that is approximately equal to or lower than that of silicon dioxide (col. 1, lines 58-60; definition of oxide film, col. 7, lines 50-55, ***Note***: the upper dielectric layer is

silicon dioxide), and the upper and lower dielectric layers together have an effective dielectric constant that is less than that of silicon dioxide.

13. Pertaining to claim 2, Fulford teaches the method, further comprising: prior to forming the lower dielectric layer, forming a trench liner **62** that substantially conforms to the trench (figure 5; col. 6, lines 50-63); wherein forming a lower dielectric layer in the trench comprises forming the lower dielectric layer over the trench liner (figure 6a; col. 7, lines 4-17).

14. Pertaining to claim 3, Fulford teaches the method, wherein the trench liner comprises silicon dioxide (col. 6, lines 50-63).

15. Pertaining to claim 4, Fulford teaches the method, wherein the thickness of the upper dielectric layer is less than the thickness of the lower dielectric layer (figure 9a; col. 8, lines 9-18).

16. Pertaining to claim 5, Fulford teaches the method, wherein the effective dielectric constant corresponds to at least one of horizontal and vertical capacitance associated with the isolation structure (col. 1, lines 55-67; col. 2, lines 1-9 ***Note***: that the prior art taught by Fulford, teaches that capacitance is directly proportional to the dielectric constant. Therefore, based on the teachings of Fulford, it is inherent that effective dielectric constant corresponds to at least one of horizontal and vertical capacitance)

17. Pertaining to claim 10, Fulford teaches the method, wherein the upper dielectric layer has a higher dielectric constant than the lower dielectric layer (col. 1, lines 58-60; definition of oxide film, col. 7, lines 50-55, ***Note***: that since the lower dielectric layer is made of a Low-K material, and the upper layer is silicon dioxide, it is concluded that the upper dielectric layer has a higher dielectric constant than the lower dielectric).

18. Pertaining to claim 11, Fulford teaches the method, wherein the lower dielectric layer has a dielectric constant below 3.9 (col. 7, lines 15-19).

19. Pertaining to claim 12, Fulford teaches the method, wherein the lower dielectric layer has a dielectric constant that is approximately 2.5 (col. 7, lines 15-19).

20. Pertaining to claim 13, Fulford teaches the method, wherein the upper dielectric layer is amorphous SiC or silicon dioxide (col. 1, lines 58-60; definition of oxide film, col. 7, lines 50-55, ***Note***: the upper dielectric layer is silicon dioxide).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fulford, Jr. et al. US Patent 6,008,109 in view of Ngo et al., US Patent US 6,797,652.

23. Fulford discloses the semiconductor method substantially as claimed. See the preceding rejection of claims 1-5 and 10-13 under 35 U.S.C. 102(b).

24. However, Fulford fails to show, pertaining to claim 6, the method, wherein the dielectric constant of the upper layer is approximately 5.0. In addition, Fulford fails to show, pertaining to claim 14, the method, wherein forming the upper dielectric layer comprises: applying an alkysilane base precursor with PECVD or an Ozone assisted technique to form the amorphous SiC.

25. Ngo teaches, in figures 1-5, and corresponding text, pertaining claims 6 and 14, a semiconductor device that uses a low-k silicon carbide dielectric layer, formed by PECVD, having a dielectric constant of 5.0, as a capping layer (col. 3, lines 48-65; col. 7, lines 35-40; col. 8, lines 4-43).

26. It would have been obvious to one of ordinary skill in the art to substitute, the method, wherein the dielectric constant of the upper layer is approximately 5.0; and the method, wherein forming the upper dielectric layer comprises: applying an alkysilane base precursor with PECVD or an Ozone assisted technique to form the amorphous SiC, in the method of Fulford, pertaining to claims 6 and 14, according to the teachings of Ngo, with the motivation that, the dielectric layer, taught by Ngo, is a silicon carbide dielectric layer, deposited by PECVD, having dielectric constant of 5.0, where this particular dielectric material is known for its improved adhesion qualities, making this dielectric material more reliable for insulation. In addition, this dielectric material is primary used for the purpose of significantly increasing electro-migration resistance. Therefore, it would be more desirable to one of ordinary skill in the art use this dielectric layer in an isolation structure, for the purpose of creating a more reliable isolation structure between the semiconductor devices, one that significantly reduces electro-migration between the active regions of the devices.

27. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fulford, Jr. et al. US Patent 6,008,109 in view of Loboda et al. US Patent 6,159,871.

28. Fulford discloses the semiconductor method substantially as claimed. See the preceding rejection of claims 1-5 and 10-13 under 35 U.S.C. 102(b).

29. However, Fulford fails to show, pertaining to claim 7, the method wherein the lower dielectric layer is Carbon doped silicon dioxide. In addition, Fulford fails to show, pertaining to claim 8, the method wherein, the Carbon doped silicon dioxide is SiOC. Finally, Fulford fails to show, pertaining to claim 9, the method, wherein forming a lower dielectric layer comprises: depositing the Carbon doped silicon dioxide by a hydrogen-peroxide assisted process, Ozone assisted deposition or organic spin-on material.

30. Loboda teaches, in corresponding text, pertaining to claims 7-9, a method for producing a H:SiOC Low-k dielectric material with a dielectric constant of 3.0 or less for the use semiconductor devices, formed by both hydrogen-peroxide and ozone assisted deposition techniques (col. 2, lines 10-22; col. 4, lines 14-23).

31. It would have been obvious to one of ordinary skill in the art to, substitute, the method wherein the lower dielectric layer is Carbon doped silicon dioxide; the method wherein, the Carbon doped silicon dioxide is SiOC; the method, wherein forming a lower dielectric layer comprises: depositing the Carbon doped silicon dioxide by a hydrogen-peroxide assisted process, Ozone assisted deposition or organic spin-on material, in the method of Fulford, pertaining to claims 7-9, according to the teachings of Loboda, with the motivation that, the dielectric layer, taught by Loboda, are generally used in the formation of semiconductor devices, where the dielectric constant is 3.0 or less. Therefore, it would be more desirable to one of ordinary skill in the art use this dielectric layer in an isolation structure, for the purpose of creating a more reliable isolation structure between the semiconductor devices, one that has a significantly reduced dielectric constant, creating a reduction of capacitance between active devices.

32. Claims 15-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fulford, Jr. et al. US Patent 6,008,109 in view of Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, Volume I, Lattice Press, 1989, pages 520-535.

33. Fulford discloses the semiconductor method substantially as claimed. See the preceding rejection of claims 1-5 and 10-13 under 35 U.S.C. 102(b). In addition, Fulford shows, pertaining to claim 19, the method, wherein the information includes vertical and horizontal capacitances associated with the isolation structure (col. 1, lines 55-67; col. 2, lines 1-9 Note: that the prior art taught by Fulford, teaches that capacitance is directly proportional to the dielectric constant. Therefore, based on the teachings of Fulford it is inherent that effective dielectric constant corresponds to at least one of horizontal and vertical capacitance).

34. However, Fulford fails to show, pertaining to claim 15, the method, wherein the upper dielectric layer has a higher or equal etch rate resistance to wet HF etch. In addition, Fulford fails to show, pertaining to claim 16, the method wherein the upper dielectric layer has an HF etch selectivity of between approximately 5:1 and approximately 30:1 to SiO2. Also, Fulford fails to show, pertaining to claim 17, the method further comprising : ascertaining a thickness of the lower dielectric layer and a thickness of the upper dielectric layer to be formed from information indicating an effective dielectric constant corresponding to relative thickness of a lower dielectric material for the lower dielectric layer and an upper dielectric material for the upper dielectric layer. Fulford fails to show, pertaining to claim 18, the method, wherein the information is obtained from an equation or graph. In addition, Fulford fails to show, pertaining to claim 20, the method, wherein ascertaining a thickness of the lower dielectric layer and a thickness of the upper dielectric layer to be formed comprises: selecting the lower dielectric

material and the upper dielectric material; selecting the effective dielectric constant, the effective dielectric constant corresponding to thickness of both the lower dielectric material and the upper dielectric material; and determining the thickness of the lower dielectric layer and the thickness of the upper dielectric layer from the information indicating an effective dielectric constant corresponding to thickness of both the lower dielectric material for the lower dielectric layer and the upper dielectric material for the upper dielectric layer. Also, Fulford fails to show, pertaining to claim 21, the method, wherein ascertaining a thickness of the lower dielectric layer and a thickness of the upper dielectric layer to be formed comprises: selecting the lower dielectric material and the upper dielectric material; selecting a range of acceptable effective dielectric constants that correspond to thickness of both the lower dielectric material and the upper dielectric material; and determining a range of acceptable thickness of both the lower dielectric layer and the upper dielectric layer form the range of acceptable dielectric constants using the information indicating an effective dielectric constant corresponding to thickness of both the lower dielectric material for the lower dielectric layer and the upper dielectric material for the upper dielectric layer. Fulford fails to show, pertaining to claim 22, the method, further comprising: determining a desired combined thickness of both the lower dielectric layer and the upper dielectric layer; selecting a thickness of a first layer of a group consisting of the lower dielectric layer and the upper dielectric layer; and ascertaining a thickness of a second layer of the group consisting of the lower dielectric layer and the upper dielectric layer from both the thickness of the first layer and the desired combined thickness. In addition, Fulford fails to show, pertaining to claim 23, the method, comprising: selecting a lower dielectric material for the lower dielectric layer and an upper dielectric material for the upper dielectric layer;

ascertaining the effective dielectric constant from information indicating the effective dielectric constant corresponding to thickness of both the lower dielectric material for the lower dielectric layer and the upper dielectric material for the upper dielectric layer; and determining whether the effective dielectric constant is within a desired range of dielectric constants. Also, Fulford fails to show, pertaining to claim 24, the method, further comprising: repeating the steps of selecting the thickness of the lower dielectric material and ascertaining the thickness of the upper dielectric material. Finally, Fulford fails to show, pertaining to claim 25, the method, wherein the upper dielectric layer has an HF rate that is lower than that of the lower dielectric layer.

35. Wolf teaches, on pages 520-535, conventional wet etching techniques, as well as selection of thickness of films that are well known in the art of semiconductor manufacturing.

36. It would have been obvious to one of ordinary skill in the art to incorporate: the method, wherein the upper dielectric layer has a higher or equal etch rate resistance to wet HF etch; the method wherein the upper dielectric layer has an HF etch selectivity of between approximately 5:1 and approximately 30:1 to SiO2; the method, wherein the upper dielectric layer has an HF rate that is lower than that of the lower dielectric layer, in the method of Fulford, pertaining to claims 15, 16 and 25, according to the teachings of Wolf, with the motivation that, conventional etching techniques, are well known in the art of semiconductor device manufacturing, as a result, determination of etch rate, film thickness, etc. would result in routine experimentation.

37. It would have been obvious to one of ordinary skill in the art, to incorporate, the method further comprising: ascertaining a thickness of the lower dielectric layer and a thickness of the upper dielectric layer to be formed from information indicating an effective dielectric constant corresponding to relative thickness of a lower dielectric material for the lower dielectric layer

and an upper dielectric material for the upper dielectric layer; the method, wherein the information is obtained from an equation or graph; the method, wherein ascertaining a thickness of the lower dielectric layer and a thickness of the upper dielectric layer to be formed comprises: selecting the lower dielectric material and the upper dielectric material; selecting the effective dielectric constant, the effective dielectric constant corresponding to thickness of both the lower dielectric material and the upper dielectric material; and determining the thickness of the lower dielectric layer and the thickness of the upper dielectric layer from the information indicating an effective dielectric constant corresponding to thickness of both the lower dielectric material for the lower dielectric layer and the upper dielectric material for the upper dielectric layer; the method, wherein ascertaining a thickness of the lower dielectric layer and a thickness of the upper dielectric layer to be formed comprises: selecting the lower dielectric material and the upper dielectric material; selecting a range of acceptable effective dielectric constants that correspond to thickness of both the lower dielectric material and the upper dielectric material; and determining a range of acceptable thickness of both the lower dielectric layer and the upper dielectric layer form the range of acceptable dielectric constants using the information indicating an effective dielectric constant corresponding to thickness of both the lower dielectric material for the lower dielectric layer and the upper dielectric material for the upper dielectric layer; the method, further comprising: determining a desired combined thickness of both the lower dielectric layer and the upper dielectric layer; selecting a thickness of a first layer of a group consisting of the lower dielectric layer and the upper dielectric layer; and ascertaining a thickness of a second layer of the group consisting of the lower dielectric layer and the upper dielectric layer from both the thickness of the first layer and the desired combined thickness; the method,

comprising: selecting a lower dielectric material for the lower dielectric layer and an upper dielectric material for the upper dielectric layer; ascertaining the effective dielectric constant from information indicating the effective dielectric constant corresponding to thickness of both the lower dielectric material for the lower dielectric layer and the upper dielectric material for the upper dielectric layer; and determining whether the effective dielectric constant is within a desired range of dielectric constants; the method, further comprising: repeating the steps of selecting the thickness of the lower dielectric material and ascertaining the thickness of the upper, in the method of Fulford, pertaining to claims 17, 18, and 20-24, according to the combined teachings of Fulford in view of Wolf, with the motivation that, as stated in col. 6, lines 33-36; col. 7, lines 24-63, the depth of the shallow trench and the selective etch, taught by Fulford, in addition, as stated on pages 520-535, the conventional techniques taught by Wolf, would lead to one of ordinary skill in the art to believe that a procedure for the determination of desired thicknesses of the upper and lower dielectric layers would be required. As a result, the determination with regards to the thicknesses of the dielectric layers, etch rate, dielectric constant etc. would result in routine experimentation in the art of semiconductor device manufacturing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
January 28, 2005

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TC 2800, AU 2812